



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/775,290 | 02/10/2004 | Yuan-Hung Liu | TSM03-0649 | 1174 |
| 25962 | 7590 | 09/26/2005 | EXAMINER | |
| SLATER & MATSIL, L.L.P. 17950 PRESTON RD, SUITE 1000 DALLAS, TX 75252-5793 | | | LEE, CALVIN | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2818 | |
| DATE MAILED: 09/26/2005 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/775,290

Applicant(s)

LIU et al.

Examiner

Lee, Calvin

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2005 (Election).
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) 11-20, 31-40 and 51-60 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 21-30 and 41-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>2/10/04</u> . | 6) <input type="checkbox"/> Other: _____ |

OFFICE ACTION

Response to Election

1. The amendment of claims 6 and 26, in the Response to Election dated September 2, 2005, is acknowledged. The Applicant's argument that "there is no alternately method of forming the spacer in claim 1 other than to 'provide' a first spacer insulating layer and to 'provide' a second spacer insulating layer" is persuasive. Therefore, claims 11-20, 31-40, and 51-60 are withdrawn from further consideration. And claims 1-10, 21-30, and 41-50 are subjected for the rejections below.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 (b) that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 41-42, 44-47, and 49-50 are rejected under 35 U.S.C. 102(e) as anticipated by *Liu* (US 2005/0136676).

- a) In re claims 41 and 46, *Liu* '676 teaches a method of forming a coupling spacer **136a** [Fig. 16 and ¶ 0038] for use with a split gate flash memory cell on a substrate having a substrate insulating layer thereon comprising a conductive layer **136** [¶ 0037] that extends between a floating gate **124a** and the substrate insulating layer **108** adjacent a source **160** recessed into the substrate **104** of the memory.
- b) In re claims 42 and 47, *Liu* suggests the conductive layer **136** being a doped polycrystalline silicon [¶ 0037].
- c) In re claims 44 and 49, *Liu* suggests the coupling spacer **136a** is located proximate a composite floating gate spacer **168** of the split gate flash memory cell [¶ 0043].
- d) In re claims 45 and 50, *Liu* teaches the coupling spacer **136a** underlying a contact spacer **144** [¶ 0040] (please see a portion of the inter-layer dielectric **144** covering the curved site of the coupling spacer **136a** and located between two adjacent coupling spacers **136a** in Fig. 16).

Liu teaches or suggests the contact spacer **144** being a composite contact spacer because *Liu* discloses the spacer material comprising oxynitride beside oxide, nitride, and metal oxide [¶ 0040].

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having skills in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 43 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Liu*.

Liu suggests the doped polycrystalline silicon layer **136** having a thickness of between 800Å and about 1200Å, but not a thickness of about 200Å.

It would have been an obvious matter of design choice to have the claimed layer' thickness (i.e., around 200Å, as suggested by *Hsieh et al* also), since such a modification would have involved a mere change in the size of the memory spacer. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

6. Claims 21-23 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Liu* in view of *Tseng et al* (US 2003/0181053), and further in view of *Hsieh et al* (US 2002/0093044).

a) In re claims 21, 23, 26, and 28, *Liu* discloses the composite contact spacer **144** [¶ 0040], but not a spacer comprising a second spacer insulating layer on a first spacer insulating layer.

Nevertheless, such multi-layer spacer is known in the semiconductor processing art as evidenced by *Tseng et al* disclosing a memory cell with triple spacers **510, 520, 720** [Fig. 7 and ¶ 0026]. It would have been obvious to one having skills in the art to have modified the composite contact spacer of *Liu* by utilizing multi-layer spacer for the purpose of stopping the diffusion of mobile ions into the floating gate(s), thereby providing an enhanced programming speed of the flash memory cell.

However, the combination of *Liu* and *Tseng et al* does not teach or suggest "a second spacer insulating layer overlying a first spacer insulating layer and having a varying deposition distribution across a surface thereof, the second spacer insulating layer having a thinner composition in selected regions of the split gate flash memory cell."

Hsieh et al describes, “a single patterned silicon nitride barrier dielectric layer **18** formed upon the blanket inter-gate electrode dielectric layer **12c** [¶ 0038]. Fig. 2 in *Hsieh et al* discloses a second spacer insulating layer **18** overlying a first spacer insulating layer **12c**, wherein the first spacer insulating layer **12c** has a substantially uniform deposition distribution across a surface being covered and the second spacer insulating layer **18** has a varying deposition distribution across a surface (i.e., having a thinner composition in a narrow region between composite floating gate spacers **16a**, **16b** of the split gate flash memory cell) [please see the even thickness of layer **12c** compared to the uneven thickness of layer **18** in Fig. 3].

It would have been obvious to one having skills in the art to have modified the composite contact spacer of *Liu* by utilizing “a second spacer insulating layer overlying a first spacer insulating layer and having a second deposition distribution that varies in substantial opposition to said first deposition distribution of the first spacer insulating layer” for the purpose of easily patterning the layers in a subsequent step of forming a composite spacer out from the two layers.

b) In re claims 22 and 27, *Hsieh et al* also suggests the composite contact spacers **12c**, **18** proximate the composite floating gate spacers **16a**, **16b** of the split gate flash memory cell [Fig. 5].

7. Claims 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Liu*, *Tseng et al*, and *Hsieh et al* ‘044 in view of *Hsieh et al* (US 5,879,992).

Hsieh et al ‘044 suggests the first spacer insulating layer **12c** formed by a dielectric layer of SiN [¶ 0032]. None of the cited arts so far suggests a spacer layer of an HTO (hot temperature oxide) layer. *Hsieh et al* ‘992 suggests [Abstract] a split gate flash having a spacer formed of HTO.

It would have been obvious to one having skills in the art to have modified the material of *Liu* 's spacer by utilizing a spacer of HTO for the purpose of having an improved spacer that is able to withstand high temperature in subsequent anneal treatment process steps (if required).

8. Claims 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Liu*, *Tseng et al*, and *Hsieh et al* '044, in view of *Yang* (US 6,875,658).

Hsieh et al ' 044 suggests the second spacer insulating layer **18** formed by a dielectric layer of SiN [¶ 0038]. None of the cited arts suggests a spacer layer of an RPO (resist protect oxide) layer. *Yang* suggests a "resist protection oxide layer adjacent to the spacer" [col. 6, ln.25].

It would have been obvious to one having skills in the art to have modified the material of *Liu* 's spacer by utilizing a spacer layer of RPO for the purpose of having an improved spacer that is able to block a subsequent implantation process step (if required).

9. Claims 1-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Liu*, *Tseng et al*, and *Hsieh et al* '044, in view of *Korovin et al* (US 6,790,123).

a) In re claims 1 and 6, *Liu* discloses the composite contact spacer **144** [¶ 0040], but not a spacer comprising a second spacer insulating layer on a first spacer insulating layer. Nevertheless, such multi-layer spacer is known in the semiconductor processing art as evidenced by *Tseng et al* disclosing a memory cell with triple spacers **510**, **520**, **720** [Fig. 7 and ¶ 0026]. It would have been obvious to one having skills in the art to have modified the composite contact spacer of *Liu* by utilizing multi-layer spacer for the purpose of stopping the diffusion of mobile ions into the floating gate(s), thereby providing an enhanced programming speed of the gate flash memory cell.

However, the combination of *Liu* and *Tseng et al* does not teach or suggest “a second spacer insulating layer overlying a first spacer insulating layer and having a varying deposition distribution across a surface thereof, the second spacer insulating layer having a thinner composition in selected regions of the split gate flash memory cell.” *Hsieh et al* describes, “single patterned silicon nitride barrier dielectric layer **18** formed upon the blanket inter-gate electrode dielectric layer **12c**” [¶ 0038]

b) In re claims 3-4 and 8-9, Fig. 2 in *Hsieh et al* discloses a second spacer insulating layer **18** overlying a first spacer insulating layer **12c**, wherein the first spacer insulating layer **12c** has a substantially uniform deposition distribution across a surface and the second spacer insulating layer **18** has a varying deposition distribution across a surface. In other words, the first spacer insulating layer **12c** has a thicker composition proximate a center of the substrate and a thinner composition toward an edge of the substrate and the second spacer insulating layer **18** has a thinner composition proximate the center of the substrate and a thicker composition toward the edge of the substrate.

It would have been obvious to one having skills in the art to have modified the composite contact spacer of *Liu* by utilizing “a second spacer insulating layer overlying a first spacer insulating layer and having a second deposition distribution that varies in substantial opposition to said first deposition distribution of the first spacer insulating layer” for the purpose of easily patterning the layers in a subsequent step of forming a composite spacer out from the two layers.

However, the combination of *Liu*, *Tseng et al*, and *Hsieh '044* does not teach “a second spacer insulating layer overlying a first spacer insulating layer and having a second deposition distribution that varies in substantial opposition to said first deposition distribution of the first spacer insulating layer as a function of the location of the split gate flash memory cell on the substrate.” Nevertheless, such deposition distribution as a function of location is known in the semiconductor processing art as evidenced by *Korovin et al* teaching the thickness variation of a deposited layer as a function of location being deposited [Fig. 1]. Moreover, “the height of the peaks 18, 20, 22 or the depth of the valleys 24, 26 in the distribution will change with the thickness of the deposited film” [col. 3].

It would have been obvious to one having skills in the art to have modified the layer formation of *Liu* by utilizing the claimed “second deposition distribution that varies substantially opposition to the first deposition” because one would control the thickness profile of a deposited layer as a function of location by modifying the surface topology of a deposited layer [Abstract] so that it has a desired thickness at various locations. In the invention case, the thinner the underlying first spacer insulating layer the thicker the second spacer insulating layer being deposited thereon.

c) In re claims 2 and 7, *Hsieh et al* also teaches the composite spacer being also a composite floating gate spacer 16a, 16b proximate a floating gate 14a, 14b of the flash memory cell [Fig. 3].

10. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Liu*, *Tseng et al*, and *Hsieh et al '044*, in view of *Bronner et al* (US 6,063,657) or *Sung* (US 6,165,843).

Tseng et al ' 053 discloses the oxide layer **610** being a TEOS-SiO₂ [Fig. 6 and ¶ 0027]. None of the cited arts above suggests a first spacer-insulating layer formed by an LPTEOS (low pressure tetraethyl orthosilicate) layer and a second spacer-insulating layer formed by a PETEOS (plasma enhanced tetraethyl orthosilicate) layer. *Bronner et al* discloses, "the spacer may be ... PETEOS ..." [col. 2, ln.65]. Alternately, *Sung* discloses, "the oxide layer **142** would be ... LPTEOS ..." [col. 4, ln.30]. It would have been obvious to one having skills in the art to have modified the spacer material of *Liu* by utilizing a insulating spacer of LPTEOS (or PETEOS) for the purpose of providing an etch mask having a conformal layer thickness [col. 4 in *Sung*].

Contact Information

11. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30 (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The central fax number for the organization (where this application is assigned to) is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at <http://pair-direct.uspto.gov>. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.



Calvin Lee

September 19, 2004